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VOLUME CONTROL DEVICE
[Onryou chousei souchi]

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Specification /1*

Title of the Invention Volume Control Device

Claim

A volume control device characterized by being equipped with a plurality of volume control means that are independently adjustable, a main volume control means interlocked with the above plurality of volume control means,

a first storage region for storing the control amounts of the plurality of volume control means, and

a saturation or zero state detecting means for detecting the saturated or zero states of the control amounts of the plurality of volume control means,

and characterized by the saturated or zero states of the plurality of volume control means being detected by the saturated or zero state detecting means and then stored in a second storage region during the adjusting of the main volume control means.

Detailed Description of the Invention

[Field of the Invention]

The present invention relates to a volume control device suitable for use in an amplifying circuit equipped with multiple power amplifiers.

[Outline of the Invention]

The present invention relates to a volume control device suitable for use in an amplifying circuit equipped with multiple power amplifiers, and is equipped with a plurality of volume control means capable of

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* Numbers in the margin indicate pagination in the foreign text.

independent adjusting, a main volume control means interlocked with the plurality of volume control means, first storage regions in which the control amounts of the plurality of volume control means are stored, and a saturated or zero state detecting means which detects the saturated or zero states of the plurality of volume control means. During the adjusting of the main volume control means, the saturated or zero states of the plurality of volume control means are detected by the saturated or zero state detecting means and are stored in a second storage region. By this, changes can be made based on a control amount that conforms to the initial set values of the plurality of volume control means.

[Related Art]

Conventionally, the playback speaker system in a satellite receiver, audio video (AV) amplifier, etc. is set up in a multidimensional manner. For example, a surround system or the like has five power amplifiers for driving the left and right front and rear speakers as well as a central speaker, and each of them is equipped with a variable resistor for volume control. Furthermore, the volumes of the front left speaker and rear left speaker, for example, can be controlled independently by means of /2 the variable resistors of the respective power amplifiers, but by turning the variable resistor of the main volume control means, the above-described front and rear speakers on the left, the variable resistors of which are interlocked with each other, can be commonly controlled.

[Problem that the Invention is to Solve]

It will be assumed that, in the above-described conventional structure, the volumes of the volume control variable resistor (henceforth

FL-VR) and volume control variable resistor (henceforth RL-VR) which are provided to the amplifiers that drive the speaker (henceforth FL-SP) located on the left front and the speaker (henceforth RL-SP) located on the left rear, respectively, are set as indicated in Figure 6A in advance. Next, if the variable resistor 8f of the main volume control means, which is interlocked with these FL-VR and RL-VR, is turned clockwise as indicated by the arrow in Figure 6A, FL-VR and RL-VR will reach the saturation point 2, at which the volumes are at their maximum, after being turned by about 300° as indicated in Figure 6B. As indicated by Figure 6B, by turning the variable resistor 8f for the main volume control counterclockwise as indicated by the arrow in Figure 6B from the condition mentioned in the above, the volumes of FL-VR and RL-VR will change to zero at the same ratio 3 as indicated in Figure 5C, regardless of the ratio that was set in advance as in Figure 6A.

For this reason, when the variable resistor 8f of the main volume control means is set to the maximum, the set values of the multiple independent variable resistors will be different from the initially set values, and the multiple initial values of the independent RL-VR and FL-VR need to be reset, which is troublesome.

The above example illustrates a case in which the main volume control means is shifted to the saturation value, but even if it is shifted to zero instead, changes will occur at the same ratio thereafter.

The present invention was devised in order to solve the above problem, and its aim is to provide a volume control device in which default settings are automatically restored by storing the set values in advance.

[Means for Solving the Problem]

As illustrated in the example of Figure 1 and Figure 2, a volume control device of the invention is equipped with a plurality of volume control means, 8a - 8e, capable of independent adjusting, a main volume control means, 8f, interlocked with the plurality of volume control means, 8a - 8e, first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR, in which the control amounts of the plurality of volume control means, 8a - 8e, are stored, and a saturated or zero state detecting means 13 which detects the saturated or zero states of the plurality of volume control means, 8a - 8e. During the adjusting of the main volume control means 8f, the saturated or zero states of the plurality of volume control means, 8a - 8e, are detected by the saturated or zero state detecting means 13 and are stored in a second storage region 7CD.

[Operation of the Invention]

According to the volume control device of the invention, the initial values of the plurality of independent volume control means interlocked with the main volume control means will not change even if the control amount of the main volume control means is set to the zero or saturated state, and this eliminates the troublesome resetting of the initial settings.

[Embodiment of the Invention]

In the following, an embodiment in which the volume control device of the invention is applied to a satellite receiver will be explained by referring to Figure 1 through Figure 4.

Figure 1 is a principle drawing of the volume control device of the

invention. From among multiple pieces of audio input data, the variable volume control amount of the first volume control means, which will be described later, is stored in the first storage regions, 7FL and 7RL. In the same manner, by the second main volume control means being adjusted as described later, the variable volume control amount of the first volume control means is increased/decreased in accordance with the second main volume control means. When the value of the second main volume control means is altered, the value of the first main volume control means in the zero or saturated state is detected by the saturation or zero detecting means 13. At this time, the differences or ratios of the variable volume control amounts of the first volume control means are stored in a /3 storage region 7CD, which stores differences or ratios. When the second main volume control means is altered, the control amounts of the first volume control means will be changed based on the data in the storage region 7CD, which stores the above-described differences or ratios.

Figure 2 and the following figures illustrate a case in which high-definition audio signals from satellite broadcasting are received and listened to through a surround stereo system. High-definition audio signals are compressed in terms of bandwidth by means of a nearly instantaneous compounding differential PCM. In other words, there are mode A in which signals uniformly quantified as 15 bits via 32kHz sampling are compressed into 8 bits and sent via 4 channels, and mode B in which 48kHz 16-bit PCM signals are compressed into 11 bits and sent via 2 channels. For example, a MUSE signal having the audio of four channels multiplexed in it is converted into a 400MHz band by means of a BS converter and BS

tuner, is turned into a base band signal by the FM detection system. Then, the audio sub-carrier is extracted by a 5.75MHz BPF, is PSK-demodulated, decoded by a PCM decoder, and is divided into analog-converted front left (henceforth FL) signal, center (henceforth C) signal, front right (henceforth FR) signal, rear left (henceforth RL) signal, and rear right (henceforth RR) signal and input to input terminals, 4a - 4e, via a MUSE signal processing circuit containing a digital filter, etc. The thus divided FL, C, FR, RL, and RR signals are fed to the preamplifiers, 9a - 9e. In order to independently control the output audio of the speaker group 11 consisting of a FL-SP, RL-SP, center speaker (henceforth C-SP), front right speaker (henceforth FR-SP), and rear right speaker (henceforth RR-SP), the above preamplifier group 9 receives data from the variable resistors (henceforth group of independent digital volumes (i.e. FL-VR, C-VR, FR-VR, RL-VR, RR-VR), 8a - 8e, which are the first volume control means, and also receives setting data from the digital variable resistor (henceforth master digital volume (i.e. M-VR)), which is the second main volume control means, via a microcomputer (henceforth CPU) 5 and a digital-analog converter group (henceforth D/A), 5a - 5e.

The variable amounts of these independent data volume group consisting of FL-VR, C-VR, FR-VR, RL-VR, and RR-VR (8a - 8e) as well as M-VR (8f) are set by pressing the plus or minus button provided in an operation part 8 or commander. The volume setting values of FL-VR 8a, C-VR 8b, FR-VR 8c, RL-VR 8d, and RL-VR 8e are stored in the respective first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR. The values obtained when the above values became saturated or reached zero are stored in the

second storage region of the memory.

The outputs of the group 9 of preamplifiers, which have had their volumes adjusted, drive FL-SP 11a, C-SP 11b, FR-SP 11c, RL-SP 11d, and RR-SP 11e of the speaker group 11 via a group 10 of power amplifiers, 10a, 10b, 10c, 10d, and 10e.

In the following, the operation of the invention will be explained by referring to Figure 3 and Figure 4.

First, if FL-VR 8a, C-VR 8b, FR-VR 8c, RL-VR 8d, and RR-VR 8e inside the operation part 8 or commander (e.g. control box) are set to the setting values indicated in Figure 3A, these values become stored in the first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR, of a memory 7. In this case, all of the values of the corresponding regions, FL', C', FR', RL', and RR', of the second storage region 7CD of the memory are zero. Next, if the setting value of FL-VR 8a is plus "35" as indicated in Figure 3B, only the setting value of FL-VR 8a will be "100," which indicates the saturated condition. In this condition, the value will not become "135" beyond "100," and the value, once it reached "100," will not change even if the plus button is pressed. Needless to say, the others, C-VR 8b, FR-VR 8c, ..., can also be set independently.

Next, if the setting value of M-VR 8f is increased by "30" while leaving the group of independent data volumes, 8a - 8e, in the condition of Figure 3B, the value of FL-VR 8a in the first storage region 7FL remains "100" since it becomes saturated at "100" as indicated in Figure 3C. The value of C-VR 8b in the first storage region 7c will be "30+30=60," and the value of FR-VR 8c in the first storage region 7FR will be /4

"70+30=100" and saturated. Similarly, both of the values of RL-VR 8d and RR-VR 8e in the first storage regions, 7RL and 7RR, will be "10+30=40." At this time, all of the values in the second storage region 7CD are zero.

Next, if M-VR 3f is increased by "1" as in Figure 3D, the values of the first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR, will be "100," "61," "100," "41," and "41." In other words, 1 is added to all but the saturated values. Furthermore, since the first storage regions, 7FL and 7FR, are saturated at "100," "101-100=1" will stored as "+1" in each of the FL' and FR' regions of the second storage region 7CD.

Figure 3E illustrates a case in which the values of the group of independent data volumes, 8a - 8e, are set as indicated in Figure 3A and in which M-VR 3f is set to plus "95." The first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR, will be "70+95=165," "30+95=125," "70+95=165," "10+95=105," and "10+95=105," respectively. Since all of them will thus be more than "100," they will be saturated values. In the second storage region 7CD, all of the first storage regions, 7FL, 7C, 7FR, 7RL, and 7RR, will stop changing once they reach the value "100."

In other words, in order to make the values of the second storage region 7CD zero when the first storage regions, 7RL and 7RR, reach "105" (In reality, they become saturated at "100."), values "+60," "+20," and "+60" (i.e. "165-105=60", "125-105=20," and "165-105=60," respectively) will be stored in FL', C', and FR' regions in the second storage region 7CD.

Next, if the minus button is pressed for M-VR 8f and the value is decreased from the condition of Figure 3E by 5 as indicated in Figure

3F, each of the data values stored in FL', C', and FR' regions of the second storage region 7CD will be reduced by 5 and become "+55," "+15," and "+55," respectively, and while the values in RL' and RR' regions remain zero, the setting values of the first storage regions, 7RL and 7RR, will be decreased by 5 and become "95" and "95." Moreover, if the value of M-VR 8f is decreased by 85 from the condition of Figure 3F, all of the values in FL', C', FR', RL', and RR' regions of the second storage region 7CD will be zero as indicated in Figure 3G. The values of the first storage regions, 7FL and 7FR, will be "70," which is reached by subtracting "30" (i.e. 85-55=30) from "100"; the value of 7C will be "30," which is reached by subtracting "70" (i.e. 85-15=70) from "100." 7RL and 7RR will indicate the value "10" (i.e. 95-85=10). Similarly, if 20 is subtracted from M-VR 8f from the condition of Figure 3G, the values of the first storage regions, 7FL, 7C, and 7FR, will be decreased by 20 to "50," "10," and "50," respectively, and 7RL and 7RR will be zero. But the values of RL' and RR' regions of the second region 7CD will be changed to "-10" and "-10."

As mentioned in the above description of the CPU 6, the plus button of M-VR 8f of the operation part 8 is pressed, the saturated value (the maximum output value), "100," or the "0" state of the power amplifier group 10 or speaker group 11 is detected by the saturation or zero detecting means 13, and based on this detection output, the regions, FL', C', FR', RL', and RR', of the second storage region 7CD will store the value increased in M-VR 8f. Figure 4 illustrates one example of a flow chart of the saturation or zero detecting means 13. Figure 4 illustrates a case in which a single memory 7 performs storing instead of the first and second

storage regions sharing the task. If the volume of FL-VR is increased or decreased in the first step ST_1, the CPU 6 determines whether the volume of FL-VR was increased or decreased as in the second step ST_2.

If an increase is detected in the second step ST_2, the saturation or zero state detecting means 13 of the CPU 6 will determine whether or not all of the values, a, b, c, d, and e, have reached 100 or higher in the third step ST_3. In this case, the values, a, b, c, d, and e, are numeric values stored in the first storage regions, 7FC, 7C, 7FR, 7RL, and 7RR, of the memory 7.

Similarly, if a decrease is detected in the second step ST_2, the saturation or zero state detecting means 13 of the CPU 6 will determine whether or not all of the values, a, b, c, d, and e, have reached 0 or lower in the fourth step ST_4. In this case, if the answer is "YES" in the third or fourth step, ST_3 or ST_4, "100" or "0" is sent as data to the speakers, and the process advances to the fifth step ST_5. In this fifth step ST_5, nothing will be executed. In other words, the volumes will be inoperable. Then, the process is returned to the first step ST_1 and /5 thus shifts to the next operation.

If the answer is "NO" in the third step ST_3, the CPU 6 advances to the sixth step ST_6, in which all of the memory values, a, b, c, d, and e, will be increased by 1. Moreover, if the answer is "NO" in the fourth step ST_4, the CPU 6 will advance to the seventh step ST_7, in which all of the memory values, a, b, c, d, and e, are reduced by 1. After the sixth and seventh steps have been finished, the process is returned to the first step ST_1 and shifts to the next operation.

According to the above embodiment, if the volumes of FL-VR 8a and RL-VR 8d are set as in Figure 5A and the volume of M-VR 8f is increased in the plus direction, the volume reaches the saturation point 2 as indicated in Figure 5B. By storing the ratios or differences 1 obtained at the time of this saturated (or zero) state in each of the regions, FL', C', FR', RL', RR', etc. of the second storage region 7CD of the memory 7 and by, when lowering the volume of M-VR 8f, changing the volume based on the ratios or differences, FL-VF 8a and RL-VR 8b will change based on the variation ratio (or difference) of the volume of the initial setting as indicated in Figure 5C. Therefore, the initial settings of FL-VR 8a, RL-VR 8b, etc. will not be erased by the setting of M-VR 8f, and this eliminates the trouble of having to perform initial setting each time audio is received.

In addition, although the above embodiment illustrates a case in which a single memory is divided into multiple regions, various modifications are naturally allowed without deviating from the scope of the invention. For example, the first and second memories may be provided independently, the signals supplied to the input terminals may be volume-controlled by a multiplier while remaining digital data, or the speakers can be suitably configured as a 2-channel, 3-channel, or 4-channel system.

[Effects of the Invention]

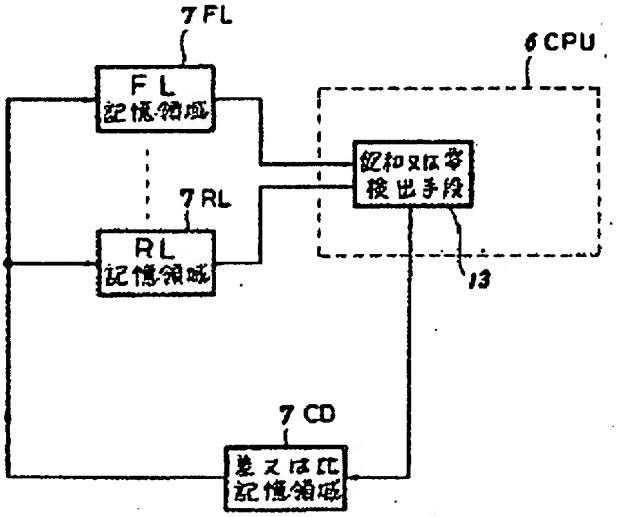
According to the volume control device of the invention, the values initially set by means of the independent variable resistors of FL-VR, RL-VR, etc. will not become erased by the setting of the master volume,

and the trouble of setting the initial values of the independent variable resistors each time audio is received can be eliminated.

Brief Description of the Drawings

Figure 1 is a principle drawing of the volume control device of the invention. Figure 2 is a general system diagram showing one embodiment of the audio control device of the invention. Figure 3 is charts for explaining the memory storage conditions of the settings of the variable resistors used in the invention. Figure 4 is a flow chart of the saturation or zero detecting means of the invention. Figure 5 is a drawing for explaining the volume control amounts of the invention. Figure 6 is a drawing for explaining the conventional volume control amounts.

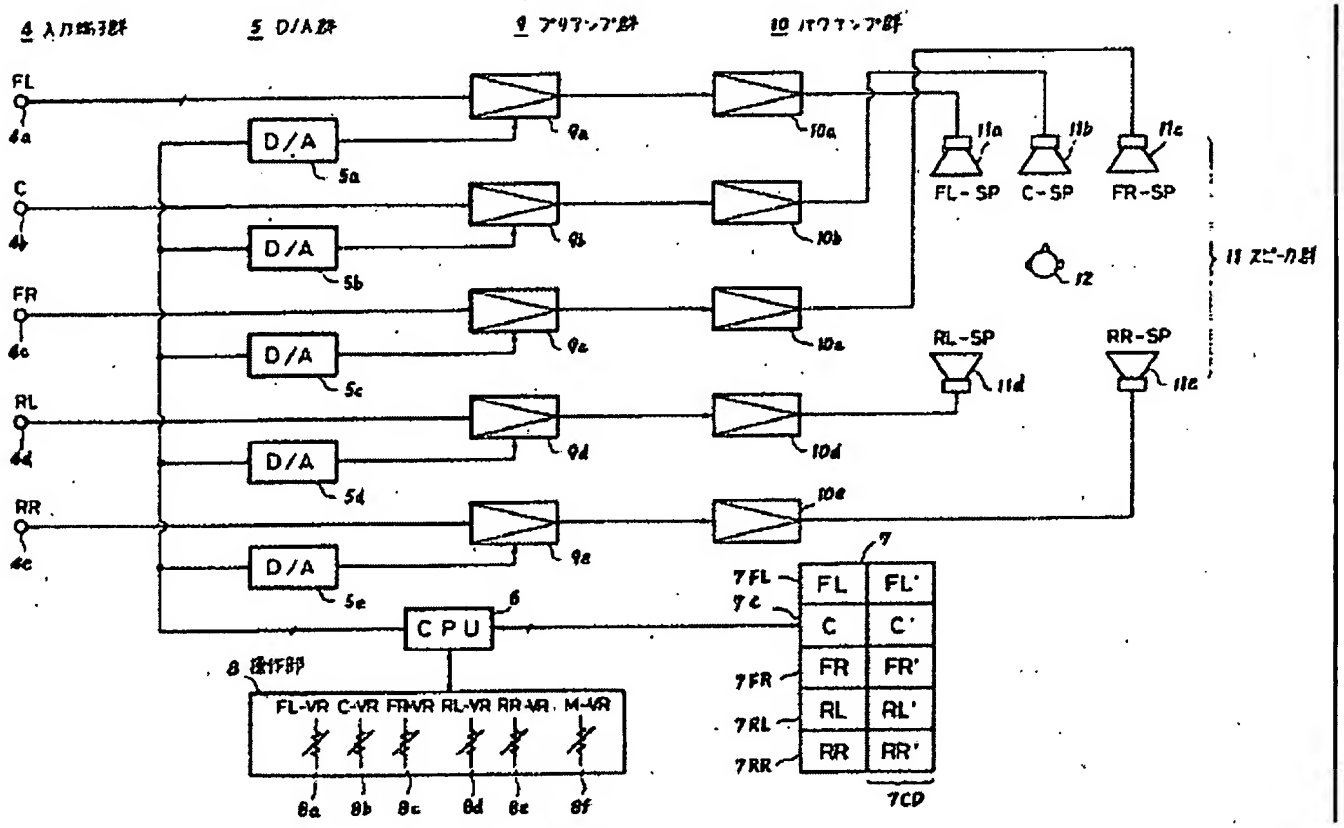
4 = input terminal group; 5 = D/A group; 6 = CPU, 7 = memory; 8 = operation part; 9 = preamplifier group; 10 = power amplifier group; 11 = speaker group.



Principle drawing of the invention

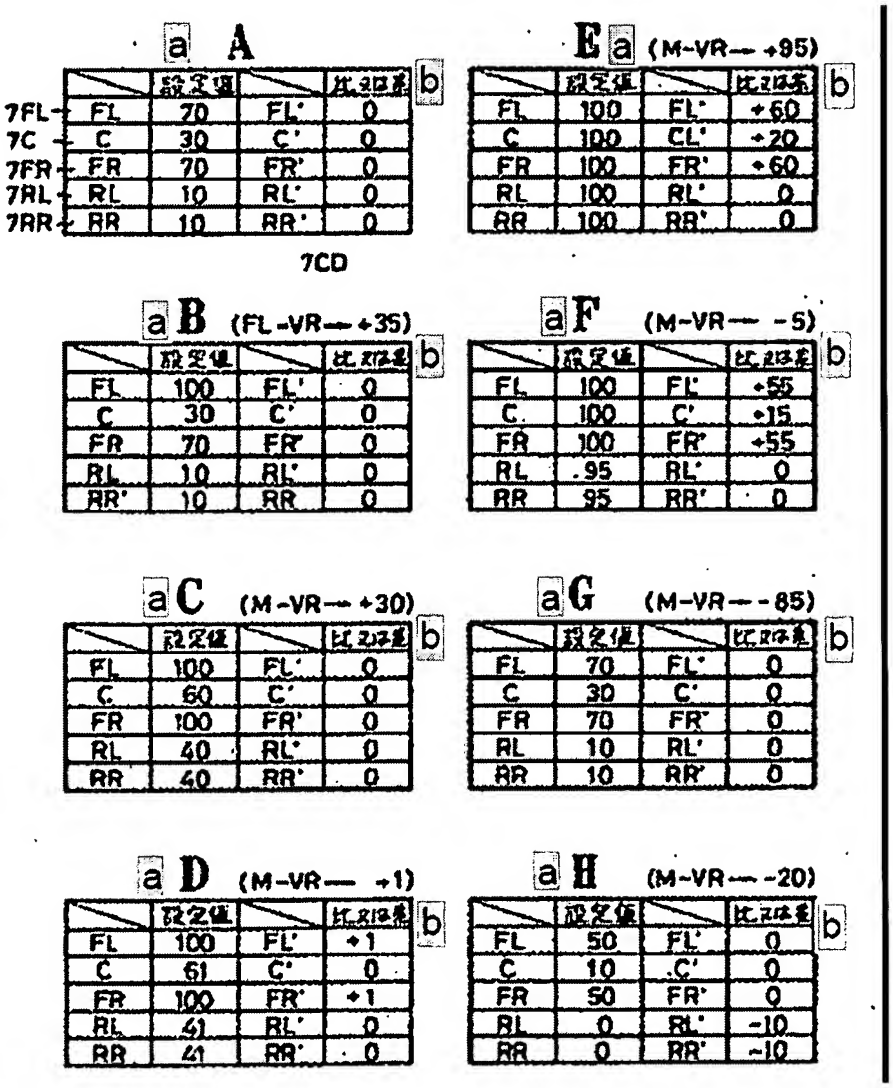
Figure 1

Key: 7FL) FL storage region; 7RL) RL storage region; 7CD) difference or ratio storage region; 13) saturation or zero detecting means.



A general system diagram showing one embodiment of the volume control device of the invention.

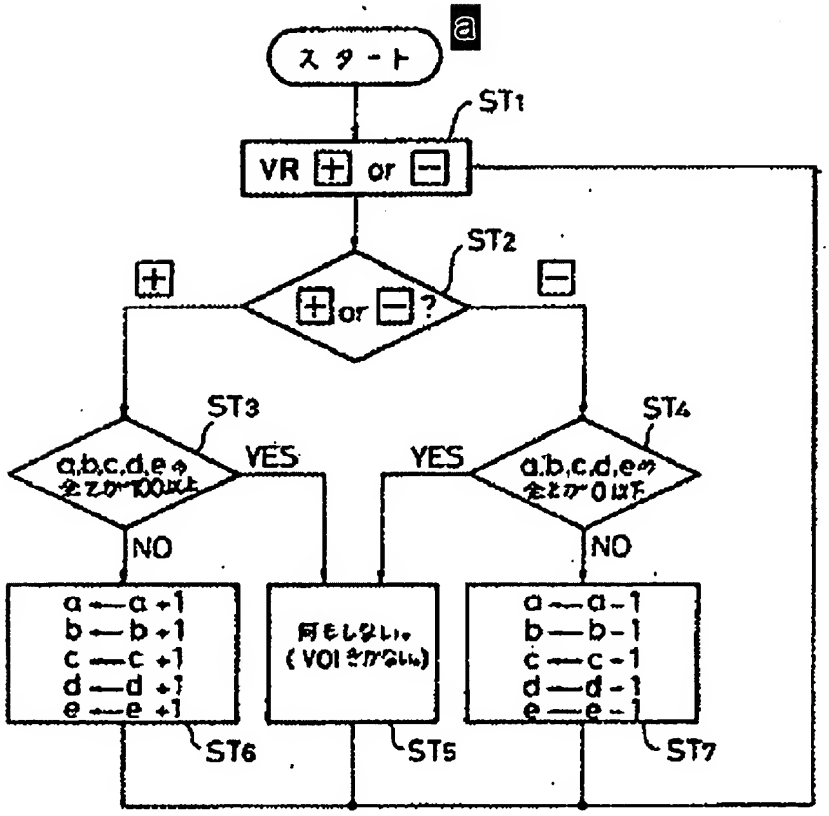
Figure 2



A drawing for explaining the storage conditions of the settings of the variable resistors.

Figure 3

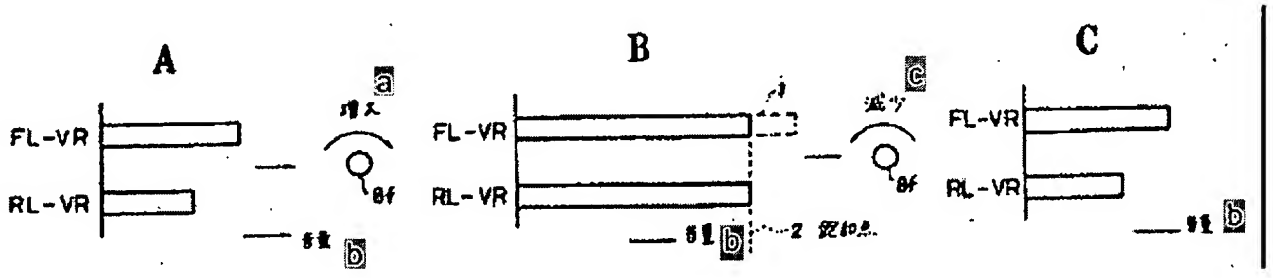
Key: a)Setting Value; b)Ratio or Difference.



A flow chart

Figure 4

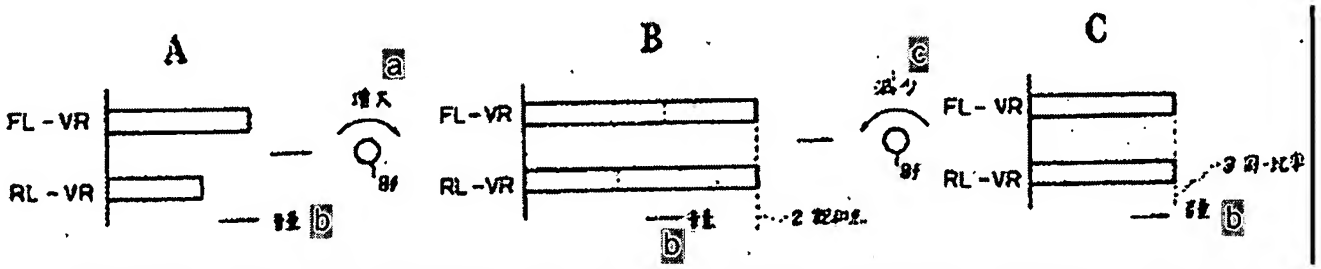
Key: a)Start; ST_3)All of a, b, c, d, and e are 100 or higher.; ST_4)All of a, b, c, d, and e are 0 or lower.; ST_5)Nothing will be executed (Volumes are not operable).



A drawing for explaining the volume control amounts of the invention

Figure 5

Key: a)increase; b)volume; c)decrease; 2)saturation point.



A drawing for explaining the conventional volume control amounts

Figure 6

Key: a)increase; b)volume; c)decrease; 2)saturation point; 3)the same ratio.